U.G. 2nd Semester Examination - 2022

COMPUTER SCIENCE

[HONOURS]

Course Code : COM.SC-H-CC-L-204

(Computer System Architecture)

Full Marks : 60 Time : $2\frac{1}{2}$ Hours

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP–A

1. Answer any **ten** questions : 2×10=20

a) How can you use a XOR gate as NOT gate?

b) State the importance of clock rate.

c) What do you mean by overflow occurrence in IEEE 754 single precision representation?

d) Implement X=(A+B)*(C/D) one-address instructions.

e) Differentiate between computer organization and computer architecture.

f) Define Latency and throughput.

g) Mention different stages of an instruction cycle.

h) What do you understand by indexed addressing mode?

i) What happens when the requested block is not present in the cache?

j) State the significance of logical addressing.

k) "Size of the program counter may be lesser than the size of address bus"– justify.

l) How stack plays an important role during interrupt processing?

m) Define memory data register (MDR).

n) Differentiate between SISD, SIMD and MIMD.

GROUP–B

2. Answer any **four** questions: 5×4=20

a) Explain the operations of DMA with the help of a neat diagram.

b) What are the limitations of the Direct Mapping? Explain how it can be improved by using set-associative mapping concept. 2+3

c) Design the common bus transfer system using Multiplexer.

d) State various functions of I/O module. Define Byte Addressability. 3+2

e) Design and implement a synchronous 3-bit up/down counter using JK flip-flops.

f) Explain Big-Endian and Little-Endian with the help of a neat diagram.

GROUP–C

3. Answer any **two** questions: 10×2=20

a) Describe the organization of a micro programmed control unit with the help of a block diagram. How does micro programmed control unit differ from hardwired control unit? 7+3

b) Why are cache replacement policies needed? Name any two cache replacement policy algorithm. A 4-way set associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. Calculate the number of bits present in block-offset, set-field, and tag-field. 3+1+6

c) Define control hazard and explain its remedies. Explain 4-bit addition using arithmetic pipelining with the help of a suitable diagram. 6+4

d) Multiply following numbers using Booth's method by clearly showing each step:

$(+14)\times(-11)$

Draw and explain 2-bit comparator circuit. 7+3

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