U.G. 3rd Semester Examination - 2024

COMPUTER SCIENCE

[MAJOR]

Course Code : CS-MJ-T-3

(Computer Organization and Architecture)

[NEP-2020]

Full Marks : 60 Time : $2\frac{1}{2}$ Hours

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP-A

1. Answer any **ten** questions : $2\times10=20$

a) Convert the hexadecimal number 3F9A to binary and decimal.

b) Explain the concept of a race condition in sequential circuits.

c) Compare a multiplexer and a decoder in terms of function and application.

d) What is the difference between a synchronous and an asynchronous counter?

e) Define and differentiate between signed magnitude and two's complement representation.

f) Explain the difference between Programmed I/O and Interrupt-Driven I/O with an example.

g) Why is Direct Memory Access (DMA) more efficient for large data transfers compared to programmed I/O?

h) What is cache coherence, and why is it important in multiprocessor systems?

i) State the role of associative memory in a Translation Lookaside Buffer (TLB)?

j) What is the significance of a tri-state buffer in bus architecture?

k) State the role of a memory address register and memory buffer register in a CPU.

l) What is the role of the MMU (Memory Management Unit) in a modern processor?

m) Differentiate between synchronous buses and asynchronous buses.

n) How does cycle stealing work in Direct Memory Access (DMA)?

o) What is cache coherence? Why is it important in multiprocessor systems?

GROUP-B

2. Answer any **four** questions : $5 \times 4 = 20$

a) Given the function $F(A,B,C,D) = \Sigma m(0,1,2,5,8,9,10,14,15)$, simplify it using Karnaugh Map (K-map) and express the result in minimum SOP form. Also draw the logic circuit using only NAND gates only for the simplified function. 3+2

b) Design a synchronous counter using D flip-flop to count the following sequence and repeat.

$1 \rightarrow 3 \rightarrow 5 \rightarrow 7 \rightarrow 11 \rightarrow 13 \rightarrow 1$ 5

c) Describe IEEE 754 single-precision floating-point representation with an example. How it differs from double-precision floating point representation. 4+1

d) A CPU follows a 16-bit instruction format, where: Opcode uses 4 bits, Register operand uses 3 bits and remaining bits are for an address or immediate value.

i) How many unique instructions can be defined using this opcode size?

ii) Explain the difference between direct addressing mode and indirect addressing mode, with examples.

iii) What is the role of a Control Memory in microprogrammed control? 2+2+1

e) Perform multiplication using Booth's Algorithm for $(-6)\times(+3)$, assuming a 5-bit binary representation. Why does Booth's Algorithm work efficiently for numbers with large consecutive 1's or 0's in the multiplier? 3+2

f) Differentiate between single-bus and - multiple-bus architectures for I/O communication. Explain how an Interrupt Service Routine (ISR) works when a keyboard generates an interrupt. 2+3

GROUP-C

3. Answer any **two** questions: $10\times2=20$

a) i) What are the main differences between RISC (Reduced Instruction Set Computer) and CISC (Complex Instruction Set Computer) architectures?

ii) Why does RISC have fixed-length instructions, while CISC uses variable-length instructions?

iii) Define Polling and explain why it is inefficient in handling I/O operations.

iv) Define the term opcode and explain its role in an instruction. 3+2+3+2

b) Consider a system which has:
Cache Size = 64 KB, Block Size = 16 Bytes, 4-Way Set Associative Mapping.

i) Calculate the total number of blocks in cache. How many sets are in the cache?

ii) If 32-bit memory address is used, then determine the Tag, Set Index, and Block Offset sizes.

iii) If memory address OxACF45D2O is accessed, determine the Set Number and Tag.

iv) Explain how Least Recently Used (LRU) replacement works in this 4-way set associative cache. 2+3+2+3

c) Discuss arithmetic pipeline with proper example. Explain the conflicts which happened in instruction pipeline. 4+6

d) i) How does bus arbitration work in a system with multiple devices?

ii) What is the role of bus width and bus speed in determining system performance?

iii) Describe any two common types of interconnection structures used in computer systems. 3+3+4
